

REMARKS*Claim Rejections Under 35 U.S.C. § 112*

Claims 1, 7, 11, 13, 17 and 20 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicant respectfully traverses this rejection.

The Examiner states that the specification does not disclose that the memory being replaced is a flash. Applicant points out that paragraph 0012 states “The embodiments of the present invention enable a single flash memory device to be replaced with multiple flash memory devices without changing the system’s memory map.” Figure 2 of the present application shows a “Logical Address Range” 210 in which the Flash RAM 200 has addresses from 00000H to 0FFFFH and 10000H to 1FFFFH. This shows a contiguous range of logical memory addresses for the flash memory being replaced. Therefore, no new matter has been introduced.

Further, the Examiner states that nowhere in the specification discloses that each flash memory devices includes a non-contiguous address sub-range. While this is an accurate statement, that is not what is being claimed or disclosed in the specification. Applicant’s claims include the limitation that “each non-contiguous address sub-range corresponds to a different one of the multiple flash memory devices” not that each memory device includes a non-contiguous address sub-range as stated by the Examiner. There is clearly a difference between these two limitations. Claim 1 has been amended to make this difference more clear. This limitation is disclosed in the present specification at Figure 2 as well as other locations.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-14, 16, 17 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Borkenhagen et al.* (U.S. Patent No. 5,067,105) in view of *Daberko* (U.S. Patent No. 5,787,445). Applicant respectfully traverses this rejection.

The combination of *Borkenhagen et al.* and *Daberko* neither teach nor suggest all of the limitations of the present claims. The combination of *Borkenhagen et al.* and *Daberko* neither teach nor suggest managing multiple memory devices that replace a single designed memory device, over a contiguous range of logical addresses, wherein each memory device is assigned to a different, non-contiguous physical address. The Examiner, in the rebuttal to Applicant’s

arguments, states that both *Borkenhagen et al.* and *Daberko* disclose flash memory. This is an accurate statement. However, the Examiner further states in the rebuttal of Applicant's arguments that each of the plurality of memory devices has a physical address sub-range as disclosed by Figure 2 of *Borkenhagen et al.* As stated previously, Applicant is not claiming that each of the plurality of memory devices has a physical address sub-range. Arguably, all memory devices have physical address sub-ranges. Applicant is claiming that "each non-contiguous physical memory address range corresponds to a different one of the multiple flash memory devices" and, further, that the multiple flash memory devices replace a single designed flash memory device over a contiguous range of logical memory addresses. These limitations are neither taught nor suggested by the combination of *Borkenhagen et al.* and *Daberko*.

Even if *Borkenhagen et al.* was modified with the flash memory of *Daberko*, the combination still does not disclose all of Applicant's claimed elements. If, as suggested by the Examiner, the cards of *Borkenhagen et al.* were replaced by the flash memory of *Daberko*, the method disclosed in *Borkenhagen et al.* would teach that physical memory selector logic 25 would operate to address the flash memory identification register 4 according to the logical memory address. The physical flash memory address would be read from the register 4 (see col. 4, lines 3 – 9). This modified combination still does not disclose Applicant's limitations that a single flash memory device is replaced by multiple flash memory devices, each with a different assigned, non-contiguous address sub-range, as presently claimed.

RESPONSE TO NON-FINAL OFFICE ACTION

Serial No. 10/624,421

Title: MULTIPLE FLASH MEMORY DEVICE MANAGEMENT

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Attorney Docket No. 400.191US01

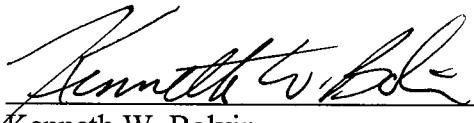
CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

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